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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :		(11) International Publication Number:	WO 98/20562
H01L 29/78, 29/10, 21/336	A1	(43) International Publication Date:	14 May 1998 (14.05.98)

(21) International Application Number: PCT/US97/17637

(22) International Filing Date: 29 September 1997 (29.09.97)

(30) Priority Data:
08/744,182 5 November 1996 (05.11.96) US

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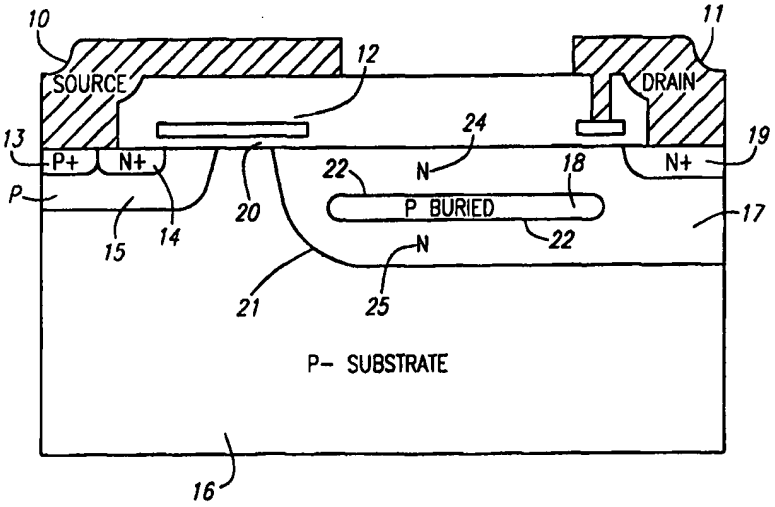
(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: HIGH-VOLTAGE TRANSISTOR WITH MULTI-LAYER CONDUCTION REGION AND METHOD OF MAKING THE SAME



(57) Abstract

A high-voltage, low on-state resistance insulated gate field effect transistor (HVFET) and method for making the same. The HVFET comprises an IGFET and a high-voltage sustaining well region. Within the well region and underneath the surface of the semiconductor channel lies a buried region. Adjacent the buried region, a plurality of conducting JFET channels are formed within the well region. The parallel conducting JFET channels provide the HVFET with a low on-state resistance. Further, a separate buried region residing in the substrate helps prevent punch-through while enabling a short-channel IGFET design. The method for making the high-voltage region of the HVFET requires only an implant and diffusion of well region of one conductivity type and implant of a buried region of another conductivity type. The method advantageously requires only two ion implants to realize the high voltage region.

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DESCRIPTION

HIGH-VOLTAGE TRANSISTOR WITH MULTI-LAYER CONDUCTION REGION AND METHOD OF MAKING THE SAME

Field of the Invention

The present invention relates to multi-layer, low on-state resistance, lateral, high voltage transistors. More specifically, the present invention relates to an improved transistor structure having the aforesaid properties, and a method for constructing the same employing a reduced amount of fabrication steps, occupying a minimal surface area, and permitting for greater manufacturing accuracy and control.

Description of Related Art

In semiconductor fabrication it is conventional to construct a high-voltage field effect transistor (HVFET) having a high breakdown voltage and a low on-state resistance in the linear region. To accomplish this end, practitioners in the art have used an insulated gate field effect transistor (IGFET) placed in series with high-voltage junction field effect transistors (JFET). Such a structure is capable of switching at high voltages, has low values of on-state resistance, and has insulated-gate control. In addition to having beneficial characteristics for various circuit applications, such a device may advantageously be fabricated adjacent low voltage logic transistors on a single integrated circuit chip.

One goal in the art is to produce a transistor with the highest breakdown voltage (Vbd) possible without degrading other features of the device. Devices having a high breakdown voltage promote superior performance in a circuit environment. The breakdown voltage of the HVFET is a function of several properties, including the charge mismatch in the semiconductor's doped layers, the length of the drain region, the magnitude of carriers in the drain region, and the level of doping in the substrate. Previous devices designed with a high breakdown voltage have been structurally large and more expensive to fabricate because they occupy more surface area on the silicon wafer.

Thus another goal in the art is to fabricate the transistors using as small a surface area as possible. A smaller HVFET transistor reduces area of the integrated circuit chip, thereby permitting the efficient fabrication of more chips on the same wafer and resulting in cost savings.

The optimal low on-state resistance HVFET, then, should have at least the following characteristics: (1) the HVFET should have the highest breakdown voltage practicable for the given surface area; and (2) the HVFET should have the lowest on-state resistance for a fixed surface area when operating in the linear region.

Another need that has arisen in the art relates to establishing a predictable, economically efficient method for fabricating low on-state resistance HVFETs. Good control over the manufacturing process is highly desirable. Traditionally, however, the fabrication techniques of such devices have been unreliable. This unreliability derives from several factors, including the large number of ion implants and thermal diffusion and oxidation steps typically required to manufacture the devices. In particular, the construction of HVFETs often necessitates several layers of diffusion, and several implant steps. The use of a large number of implant steps in fabrication can create deficiencies in device performance. For example, implant concentration increases the carrier-to-impurity center and carrier-to-surface scattering within the semiconductor layers, which in turn decreases the carriers' mobility within the conducting channels. Carrier scattering also raises the transistor's on-state resistance. In addition, because of the tolerances associated with each implant step, the use of additional implant steps increases the charge mismatches within the transistor layers.

The breakdown voltage Vbd of a semiconductor is a function of the charge mismatch within the semiconductor's diffused layers. For this reason, knowledge of, and control over, the mismatch is critical before a device having a predictable range of breakdown voltage Vbd can be fabricated. Furthermore, because tolerances associated with ion implants and thermal processes create undesirable charge mismatches between layers, it is advantageous to construct a device using a process which utilizes a minimal amount of ion implants and diffusion and oxidation steps.

As an illustration, a low resistance HVFET is typically fabricated using three

or more implant steps to realize the device's JFET structure. Naturally, the more steps used in the fabrication process, the more expensive the fabrication process becomes. Moreover, the requirement of three implants will necessarily inject a greater charge mismatch and increased carrier scattering into the device. As such, the mobility of the electrons/holes in the conducting channels is decreased. Such a decreased mobility places practical limits on how low a value of Ron may be achieved.

One proposed device uses three layers within a substrate to realize a high voltage MOS transistor with a low on-state resistance. This device is described in U.S. Patent No. 5,313,082, issued to Klas H. Eklund for *High Voltage MOS Transistor With A Low On-Resistance*. The pertinent portion of this device is shown in Fig. 1. The device is a MOS transistor having a source, drain, and insulated gate region. Connected to the drain diffusion region 24 is an N-type extended drain region 26, a P-region 27, and an N-top region 28. Together with the P-layer 27, the extended drain region 26 and the N-Top layer 27 function as a parallel, double-sided JFET having dual current channels. Advantageously, the use of dual current channels as shown lowers the on-state resistance of the transistor. Another device using three layers within a P-substrate to realize a high voltage MOS transistor is described on U.S. Patent No. 4,626,879, issued to Sel Colak. Yet another device using three layers within a P-substrate to realize a high voltage transistor is described in U.S. Patent No. 5,146,298, issued to Klas H. Eklund.

The following needs in the art exist with respect to the structure and fabrication of high voltage, low on-state resistance field effect transistors: (1) the need for an ever-smaller, low resistance HVFET, compatible on the same integrated circuit with low voltage logic; (2) the need for a HVFET having an even lower on-state resistance than previous related devices; (3) the need for a HVFET having a maximized breakdown voltage; (4) the need for a fabrication process which is simpler to achieve in a mass-production environment; and (5) the need for a fabrication process which necessitates minimum implant steps, which in turn yields enhanced manufacturing control, improved device performance, greater device predictability, and lower fabrication costs. The present invention provides a solution to the above needs.

The present invention, a high voltage low on-state resistance transistor including a parallel JFET structure, affords additional advantages over those provided by previous devices. The present invention likewise solves further problems that have arisen in the art, and provides key improvements in structure, function, and processing methodology.

Summary of the Invention

The present invention relates to a high-voltage field effect transistor structure and fabrication method which provides significant improvements over existing devices. The structure provides for a high voltage, low on-state resistance insulated gate field effect transistor. The device is structurally simpler, and easier to build, than related devices. At the same time, the device provides enhanced performance via, among other advantages, a lower on-state resistance (Ron) for the same breakdown voltage (Vdb). While n-channel high voltage FETs are presented herein for illustrative purposes, the present invention equally contemplates both an n-channel HVFET and a p-channel HVFET.

The disclosed method provides for a greatly simplified, more predictable, and less expensive fabrication technique. The method requires fewer fabrication steps than similar methods and greater control over the manufacturing process. The method is easier to control in practice.

The present invention comprises an insulated gate field effect transistor (IGFET) in series with a parallel combination of two high-voltage junction field effect transistors (JFET). A source and drain region are diffused into the semiconductor surface to form the IGFET. Connected to the drain region lies a well region comprising a first dopant type. The JFET channels extend substantially across the extended drain region and may partially underlay the IGFET gate electrode. The lower surface of the channel borders the upper surface of the substrate. Formed beneath the upper surface of the well region, but above the lower surface of the well region is a buried layer having a dopant type which is opposite to that of the well region. The well region above and below the buried layer form individual JFET current channels for transistor current conduction into the drain region. Depending on the desirable breakdown voltage and the electrical parameters

sought to be optimized, the length, width and depth of the buried layer and the well region will vary. To optimize performance of the JFET for particular circuit applications, the buried layer may also be segmented into several portions of various sizes, shapes and quantities.

The gate of the JFET structure is realized by PN junction between the buried layer and the well region. For enhanced JFET switching characteristics, the buried layer may be connected to the substrate. When the JFET is acting in the triode region of operation, the two JFET current channels act as parallel resistors. The existence of two, rather than one, JFET current channels measurably reduces the on-state resistance of the IGFET device.

The present invention further includes a method for fabricating the low on-state resistance HVFET. The method requires only two implant steps to realize the JFET structure. In the first step, the well region is implanted and diffused into the semiconductor surface. In the second step, the buried layer is created by a single, high energy implant. The magnitude of energy and concentration of impurities used in the high energy implant step is selected so as to position the buried region to a predetermined depth below the surface of the well region.

Again, depending on the application, the shape, size, and position of the buried layer will vary. In one preferred embodiment, the buried layer resides in a single diffused region and provides the double-sided JFET structure with dual current channels. In another preferred embodiment, a separate and discrete portion of the buried layer is placed substantially beneath the source. That portion of the buried layer has distinct advantages. One such advantage is to counteract the occurrence of drain-to-source punch-through while enabling the IGFET structure to be manufactured with a shorter channel length than similar devices. The other such advantage is to assist in depleting the n-well material when the transistor is in the off-state.

In still another preferred embodiment of the invention, the buried layer includes perforations for current flow between the channels of the JFET region. This preferred embodiment, like the others, provides for further improvement of on-state resistance. Still other preferred embodiments enable the manufacturer to vary the shape, size and contour of the buried layer to achieve a variety of beneficial

characteristics. These characteristics include effective three-dimensional depletion of the buried layer and the well region and a measurably reduced on-state resistance. The buried layer may also be segmented into a plurality of discrete sections to optimize circuit performance for various conditions. In short, the present invention enables the designer to vary the contour of the buried layer in a manner that optimizes the particular characteristics of greatest importance to his or her circuit application.

An object of the present invention is to provide a high voltage field effect transistor device employing a JFET structure wherein the parallel conducting JFET channels permit a very low on-state resistance, and a short IGFET channel length, thereby providing for a compact and efficient transistor structure.

Another object of the invention is to provide a high voltage, low on-state resistance transistor structure having an effective JFET gate flexibly positioned within a single well region for optimal device performance under which the maximum achievable breakdown voltage and the lowest on-state resistance may be achieved.

Another object of the invention is to permit the use of an HVFET which provides for greater immunity to device degradation problems such as punch-through between source and drain.

Another object of the invention is to provide a high voltage, low on-state resistance insulated gate field effect transistor which permits for optimal depletion in the JFET region of the device, conserving the charge matching conditions at much higher levels of charge.

Another object of the invention is to provide a method of fabrication of a high voltage transistor having an on-state resistance which is lower than that of previous similar devices.

Another object of the invention is to provide a method for producing a high voltage, low resistance transistor at a reduced fabrication cost.

Another object of the invention is to provide a more predictable method for producing a high voltage, low resistance transistor which includes optimal control of the manufacturing process, fewer impurity losses, and higher carrier mobility.

Additional objects and benefits of the present invention may be contemplated

by those skilled in the art after perusal of the specification, drawings and claims herein.

Brief Description of the Drawings

Fig. 1 depicts a prior art high voltage, low on-state resistance transistor.

Fig. 2 depicts a cross-sectional view of an improved n-channel, low on-state resistance HVFET in accordance with one embodiment of the present invention.

Fig. 3 depicts a cross-sectional view of an improved n-channel, low on-state resistance HVFET in accordance with another embodiment of the present invention.

Fig. 4 depicts an illustrative graph which shows carrier concentration as a function of distance into the semiconductor in accordance with the method of the present invention.

Fig. 5 shows a cross-sectional view of an improved n-channel high voltage, low on-state resistance IGFET in accordance with another embodiment of the present invention.

Fig. 6 shows a top, cross-sectional view of the p-buried layer of the device shown in Fig. 7, taken along plane x1x2.

Fig. 7 illustrates a top view of portions of a P-buried layer in accordance with another embodiment of the present invention.

Fig. 8 depicts a top view of portions of a P-buried layer in accordance with another embodiment of the present invention.

Fig. 9 shows a top view of a P-buried layer in accordance with another embodiment of the present invention.

Fig. 10 represents a cross-sectional view of an improved n-channel high voltage, low on-state resistance transistor in accordance with another embodiment of the present invention.

Fig. 11 depicts a cross-sectional view of an improved n-channel high voltage, low on-state resistance transistor in accordance with another embodiment of the present invention.

Figs. 12(a) and 12(b) show a top view of two exemplary P-buried layers in accordance with another embodiment of the present invention.

Fig. 13 depicts a cross-sectional view of another embodiment of the present

invention where the gate electrode overlaps the edges of the P-buried region near the source and the N^+ drain diffusion overlaps the edge of the P-buried region near the drain to facilitate current flow even if the P-buried implantation comes to the surface at the edges.

Fig. 14 depicts a cross-sectional view of another embodiment of the present invention wherein separate MOS channels are provided for each of the N-region current flow paths.

Description of the Preferred Embodiments

Referring now to Fig. 2, an exemplary n-channel high voltage, low on-state resistance HVFET transistor is shown in accordance with a preferred embodiment of the present invention. An n-channel transistor is demonstrated here. It should be understood, however, that the present invention equally contemplates an analogous p-channel transistor. The p-channel transistor may be realized by utilizing the opposite dopant types for all of the illustrated diffusion regions. The device in Fig. 2 constitutes an insulated-gate field effect transistor (IGFET) having a gate 12 (comprised, for example, of aluminum or polysilicon), an insulating layer 20 such as silicon dioxide or another appropriate dielectric insulating material, and an underlying P- substrate region 16. The gate 12, insulating layer 20 and the substrate 16 together form the insulated gate region of the device. In a preferred embodiment, the gate region is a metal-oxide semiconductor (MOS), and the IGFET is a MOS transistor.

The n-channel device also has a source contact 10 over an N+ source diffusion region 14, and a drain contact 11 over an N+ drain diffusion region 19. Preferably, adjacent the N+ source diffusion region 14 lies a P+ diffusion region 13, which increases the integrity of the source to substrate connection.

The device also contains a separate N-well region 17. The drain diffusion region 19 resides in the N-well region 17. Within the N-well region 17 lies a buried region 18 of P type. The P-buried region 18 is positioned such that it is sandwiched within the N-well region 17.

Together with the region of N-diffusion above 24 (labeled "N above" in Fig. 2) and the region of N-diffusion below 25 (labeled "N below" in Fig. 2), the P-

buried region 18 forms a double-sided, parallel-configured junction-field effect transistor. The PN junction 22 of the double-sided JFET exists around the P-buried region 18.

Preferably, the double-sided JFET acts as a voltage controlled resistor, where the JFET channel resistance is determined in part by the potential of the P-buried region 18. Under normal conditions, current flows from the source region 14 through the IGFET gate and then parallels through the N-above region 24 and the N-below region 25 to the drain region 19. Because there are two current paths, the resistance of the channel is substantially reduced. Thus, the HVFET structure of the present invention provides for a very low on-state resistance.

In a preferred embodiment, the P-buried region is not floating but instead is connected to the substrate 16 or another element having substantially the same potential (the attachment is out of the plane of Fig. 2 and is not shown). The substrate may be connected to ground. The ground connection provides the double-sided JFET with enhanced switching characteristics.

Referring back to Fig. 2, the n-channel IGFET preferably includes an additional P-region 15 into which both source regions 13 and 14 are diffused. One function of the P-region 15 is to counteract the adverse effects associated with drain-to-source punch-through. Punch-through can occur, for example, when the N-well region 17 becomes excessively depleted as the drain-to-source voltage (Vds) of the HVFET increases. In such a case, the depletion region formed at the border of the n-well region 17 and the substrate 16 would tend to migrate to the left and toward the source in Fig. 2. In the present invention, the depletion region is prevented from reaching through to the source region 14 because of the p-region 15.

The aforedescribed structure provides numerous advantages relating to semiconductor fabrication. The present invention may be fabricated using a simplified, more accurate and less costly technique than previous devices. In particular, previous structures having a similar function have often required a minimum of three separate layers, and therefore three implant steps, to realize a double-sided JFET structure. The use of three implants is not only more costly, but it also increases the charge mismatch between the layers. An increased charge mismatch presents certain limitations on device performance. For example, it

reduces the breakdown voltage of the HVFET. Excessive implants in the channel also increase the number of impurities in the channel. This increased concentration decreases the mobility of electrons and/or holes flowing through the channel, which in turn places practical limits on the device's lowest achievable on-state resistance. Additionally, the implants will tend to compensate each other, which also decreases carrier mobility due to high ionized impurity scattering.

In contrast to previous structures, the structure of the present invention requires only two implants to form the parallel JFET region of the device. The N-well region 17 in Fig. 2 is implanted and diffused in a standard manner, preferably to about 6 microns. (Where the device to be fabricated is a p-type IGFET, a P-well implantation would be substituted for the present step.) The dose, or amount of impurities should preferably be chosen in a manner consistent with having compensating effect with the p-buried layer and resulting p-charge of about that of the sum of both n-layer charges, which is about 4×10^{12} and having the top and buried n-layers with charges of about 2×10^{12} cm^{12} for each. To implement this procedure, the implant dose of n-type impurities is about 5×10^{12} cm^2.

Next, the P-buried layer 18 is implanted using a high energy implanter. The P-type dopant is preferably boron. (Where the device is a p-channel IGFET, an N-buried implant would instead be used.) The energy and dose of this P-implant are to be selected in a way that places the P-buried layer 18 inside the N-well region 17, leaving the N-above region 24 on top of the P-buried layer 18 substantially undisturbed. In a preferred embodiment, the P-buried region is implanted such that its upper surface is positioned at about 1.0 to 2.0 microns below the surface of the N-well region 17. For example, an implant dose of P buried layer may be 5×10^{12} cm^2 and the implant energy may be 800 KeV.

Fig. 4 depicts a graph which shows a typical impurity concentration for the two-implant fabrication process described above. The graph is for illustrative purposes only, and is not intended to limit the invention to the quantities described therein. The n-channel IGFET of Fig. 2 is used for this example. The vertical axis of the graph represents the ion log concentration. This quantity is measured by the number of ions per cubic centimeter. The horizontal axis of the graph represents the vertical distance (depth) into the semiconductor material (in Fig. 2, the

semiconductor material to be implanted is P- substrate 16). This quantity is measured in microns. For instance, the quantity 0.0 microns represents the surface of the semiconductor, whereas the quantity 10.0 microns represents 10.0 microns below the semiconductor surface.

The first implant step is depicted by line A. For the device in Fig. 2, the implant is of n-type material. (e.g., phosphorous, etc.) The thermal diffusion pushes the impurity inward. Of course, the deeper into the semiconductor material, the lower the concentration of n-type material. The concentration of n-type material is reduced to approximately 10^{14} ions per cubic centimeter at 10 microns below the surface. Thus, with respect to the device in Fig. 2, the n-well region 17 is formed into the substrate 16.

The second implant step is shown by line B. This implant is a high energy implant as described above. For an n-well device such as in Fig. 2, a typical p-type material is used in the implant (e.g., Boron, etc.). As illustrated by the graph, the high energy used in the implant drives the p-type material below the surface of the n-well region. The depth of the p-type material is controlled in part by the amount of energy used in the implant.

Only at about 1 micron does the concentration of p-type material begin to increase. From approximately 1 micron to 2.0 microns, the concentration of P-type material is highest and is represented by the hump of Line B. The hump represents the P-buried layer 18 in Fig. 2. After 2.0 microns, the concentration of p-type material substantially decreases to about 10^{14} ions per cubic centimeter.

In this example, the region between about 0.0 and 1.0 microns substantially represents the N-above region 24, and the region between about 2.0 and 8 microns substantially represents the N-below region 25. Similarly, the region between about 1.0 and 2.0 microns substantially represents the P-buried region 18. Using the above method, the semiconductor manufacturer may select the dimensions of all three regions by varying the amount of energy and the amount of dopants used in the implant steps.

Line C illustrates the net concentration of impurities after compensation has occurred. As evidenced by the similarity of Line C to Lines A and B, the net effect of compensation is minimal. In other words, this method provides for charge-

matching at a low n-well concentration. This advantageously results in a reduced amount of carrier scattering and other undesirable side effects associated with processes involving a greater number of implants.

The use of only two implants to fabricate the structure of the present invention has numerous advantages. First, the use of implants is generally considered in the art to be a more accurate fabrication method than epitaxial layering. Second, the use of fewer implants reduces the fabrication cost of the device. Third, the use of less implants significantly reduces the charge mismatch between layers associated with excessive implants. Additional advantages will be apparent to those skilled in the art after perusal of the instant specification, drawings and claims.

In the present invention, enhanced control of the manufacturing process may be achieved. Because only two implants are required, the charge balance within the N-well region 17 may be maintained. Additionally, the use of a single Boron implant exposes the semiconductor material to a comparably small amount of diffusion and subjects the semiconductor to a minimal period of high temperature. As such, the loss of impurities is minimal. Moreover, there exists comparably less carrier-to-dopant and carrier-to-surface scattering, which provides for an increased mobility of carriers in the channel. This advantageously results in a lower on-state resistance for the device.

Another preferred embodiment of the invention is shown in Fig. 3. The embodiment of Fig. 3 depicts an n-channel HVFET; however, a p-channel HVFET is within the scope of the present invention and can be realized by reversing the diffusion types on the various doped regions. This embodiment is similar to that illustrated in Fig. 2 in that it includes a source contact 30, source diffusion regions 33 and 34, drain contact 31, drain diffusion region 39, insulating layer 40, p-substrate 36, n-well region 37, p-buried region 38, and gate contact 32.

The structure in Fig. 3 functions in a similar manner to the structure in Fig. 2. A unique advantage of the structure in Fig. 3 is that it may be constructed with a very short IGFET channel length, which drastically reduces the device's on-state resistance. The short IGFET channel length may be attributed to the portion of the P-buried layer 35 which resides substantially beneath the source diffusion regions 33 and 34. The P-buried layer 35 in Fig. 3 provides benefits which are similar to

those provided by the P region 15 in Fig. 2. For example, the P-buried layer 35 provides effective depletion of the N-well 37 laterally, and vertically which helps prevent punch-through between the source and drain. More specifically, in Fig. 5, the P-buried layers 35 and 38 act in conjunction to pinch-off the N-well region 37 between layers 35 and 38. By pinching off the N-well region 37, the layers 35 and 38 collectively counteract the potential for source-to-drain punch-through.

Placement of the P-buried layer 35 underneath the source is advantageous. As described below, such placement enables the manufacturer to realize a high voltage, low resistance IGFET having a short channel length. A transistor having a shorter channel length occupies less surface area on a silicon wafer. Thus, the present invention provides for an increased savings of surface area per transistor, which corresponds to a more efficient design and a decreased fabrication cost.

Preferably, the P-buried layer 35 in Fig. 3 is placed substantially directly beneath the source diffusion regions 33 and 34. This placement permits a reduced channel length of the IGFET. This configuration may be contrasted with that of Fig. 2, where the P-region 15 in Fig. 3 typically extends to the right of source diffusion regions 33 and 34 and up to the surface of the semiconductor. Because the P-buried layer 35 in Fig. 3 counteracts the penetration of drain potential into the IGFET channel region, the IGFET channel length can be reduced. Thus the source diffusion regions 33 and 34 may be fabricated closer to the N-well region 37, advantageously resulting in an HVFET with a reduced IGFET channel length.

The embodiment shown in Fig. 3 can be fabricated without use of additional implant steps. For example, the P-buried layer 35 may be created using the identical implant step in which the P-buried layer 38 is created. The manufacturer need only mask out the areas on the semiconductor where placement of the P-buried layer is not desired (e.g., beneath the gate). Thus, the fabrication of the structure shown in Fig. 3 may be made with the same number of process steps as the structure of Fig. 2, while simultaneously allowing for a shorter IGFET channel length.

Another preferred embodiment of the present invention is shown in Fig. 5. The structure includes a source 50, source diffusion regions 53 and 54, drain 51, drain diffusion region 59, substrate 56, N-well region 57, and P-buried layer 55.

While an n-channel device is shown for purposes of illustration, an analogous p-channel device may also be contemplated.

In the embodiment shown in Fig. 5, the P-buried layer 55 is preferably fabricated using a single implant step similar to the previous embodiments. However, unlike the previous embodiments, the P-buried layer 55 includes openings 61. The openings 61 provide a mechanism wherein the N-above region 62 is connected to the N-below region 63 to form two JFET channels in parallel. Unlike in the previous embodiments, the N-above region 62 is connected to the N-below region 63 at a position away from the gate region. This embodiment advantageously permits the design of IGFETs having short channel lengths.

Further, the P-buried layer 55 is preferably connected to ground potential via the substrate. As previously explained, connection of the P-buried layer 55 to ground potential ensures optimal switching characteristics for the device. Also, in this preferred embodiment, the N-above region 62 is connected to the N-below region 63 at a position close to the drain diffusion region 59, which increases the HVFET breakdown voltage.

Fig. 6 depicts a cross-sectional view of the P-buried layer 55 illustrated in Fig. 5. A plurality of distinct openings in the layer 55 connect the N-above region 62 to the N-below region 63. The view in Fig. 6 represents an exemplary structure of the P-buried layer in accordance with the present invention. It should be understood, however, that other shapes, sizes, and quantities of openings may be contemplated and are within the scope of the invention. For example, the P-buried layer 55 may contain openings which are hexagonal, square, circular, triangular, or another shape. It may also contain openings which differ in size and/or shape with respect to one another.

The size of the openings 64 are preferably such that the N-well inside the region (P-well in the case of a p-channel IGFET) is pinched-off by the surrounding P-buried layer 55 at drain voltages of 20 to 100 volts. For circular openings, typical radii of the openings are 2 to 4 micrometers.

In the above embodiments, the P-buried layer 55 acts in a one-dimensional fashion to deplete the N-above and N-below regions 62 and 63. Similarly, the N-above and N-below regions act unidimensionally to deplete the P-buried layer 55.

The effective charges in these layers, however, can be increased by recognizing that the N-above region 62, P-buried region 55 and N-below region 63 can be made to deplete in a three dimensional fashion. For instance, a spherical P-buried layer can deplete n-type charges around it in a three dimensional fashion. Thus, a spherically or other shaped buried layer can be formed to make use of multi-dimensional depletions.

Additional shapes of the P-buried layer can be contemplated. For instance, Fig. 7 depicts a square pattern of P-buried layers. The layers would be formed using a conventional ion implant step and an appropriate mask. Fig. 8 illustrates P-buried layers configured in a checker-board pattern. Fig. 9 depicts a uniform P-buried layer having square shaped openings 69. Again, in a P-channel IGFET, the layers illustrated in Figs. 6-9 would be formed with N-type material. Apart from the square patterns, hexagonal patterns, or circular patterns, patterns of other geometry may comprise the P-buried layer (N-buried layer for p-channel device). Where a plurality of sections of buried layers are used, such as in Fig. 7, the sections are preferably left floating. Conversely, where the buried layer is comprised of a single section, such as in Fig. 9, the buried layer is preferably connected to ground via the substrate.

In addition to the above patterns comprising the P-buried layer of the JFET structure, alternating patterns of openings in the buried layer and the floating buried layer can be designed and are within the scope of the invention.

Another preferred embodiment is illustrated in Fig. 10. Like in the previous embodiments, this structure comprises an HVFET having a drain contact 101, a drain diffusion region 108, a source contact 100, source diffusion regions 103 and 104, substrate 107, and a buried layer 105. While the structure in Fig. 12 illustrates an n-channel HVFET, a p-channel HVFET may also be realized.

The embodiment shown in Fig. 10 differs from the previous embodiments in that the high voltage JFET transistor is formed using P+ isolation diffusion 109 and an N-epitaxial layer 106 on a P substrate 107. Preferably, the structure functions in a manner similar to the embodiment of Fig. 2. A layer of P diffusion 110 provides protection from the occurrence of drain-to-source punch-through. The P-buried layer 105 acts as an effective gate for a parallel-configured JFET having dual

current channels. Advantageously, this structure requires only a single implant 105 (i.e., a high energy P implant) to form the high-voltage sustaining region.

In addition, the preferred embodiment shown in Fig. 10 may be improved upon by implanting a P-buried layer underneath the source diffusion regions. For example, Fig. 11 discloses a structure similar to the structure shown in Fig. 10. The difference lies in the portion of the P-buried layer 210 in Fig. 11 which is implanted substantially directly beneath the source diffusion regions 203 and 204. That portion of the P-buried layer 210 preferably serves to prevent punch-through while providing for a reduced IGFET channel length. The structure in Fig. 13 is similar to the embodiment shown in Fig. 3. The structure in Fig. 11, however, is formed using a P+ isolation diffusion and an N-epitaxial layer on a P- substrate. In this structure, like the structure in Fig. 10, only a single implant is needed to form the P-buried layer 205.

Like in the previous embodiments, the structure in Fig. 11 functions as a low resistance HVFET with a reduced channel length.

When the edges of the masking material used to form the P-buried layer has too much slope, the P-buried implantation may extend to the surface at its edges 306. Fig. 13 depicts a cross-sectional view of another embodiment of the present invention where the gate electrode 302 overlaps the edge of the P-buried region near the source and the N^+ drain diffusion 308 overlaps the edge of the P-buried region near the drain to facilitate current flow across both the top and bottom portion of N-region.

Fig. 14 depicts a cross-sectional view of another embodiment of the present invention wherein separate MOS channels 403 and 404 are provided for current flow through the N-regions 424 and 425, respectively. This embodiment, because of the presence of two parallel MOS channels, may have a lower on-state resistance compared to other embodiments.

Although the present invention has been described in terms of the presently preferred embodiments, it should be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will become apparent to those skilled in the art after perusal of the present specification, drawings and claims. Consequently, it is intended that the appended claims be interpreted as

covering all such alterations and modifications as falling within the spirit and scope of the present invention.

What is claimed is:

1. A high voltage FET comprising:

a semiconductor substrate of a first conductivity type having a substrate surface;

a first region of a second conductivity type having a first surface, said first region within said substrate, said first surface bordering said substrate surface;

a second region of said first conductivity type having a second surface, said second region within said substrate and said second surface bordering said substrate surface;

a source diffusion region of said second conductivity type, said source diffusion region within said second region;

a source contact connected to said source diffusion region;

a drain diffusion region of said second conductivity type, said drain diffusion region within said first region;

a drain contact connected to said drain diffusion region;

a buried region of said first conductivity type within said first region and beneath said first surface, said buried region forming dual current channels within said first region, one channel above said buried region and another channel below said buried region;

a gate region having an insulating layer formed over said substrate surface; and

a gate electrode on a section of said insulating layer over said substrate surface, said gate electrode together with said insulating layer and said substrate forming an insulated gate having a transistor channel between said source and said first region.

2. The HVFET according to claim 1 further comprising

a third region of said first conductivity type within said second region and adjacent said source diffusion region.

3. The HVFET according to claim 1 wherein said buried region adjoins said drain diffusion region.

4. The HVFET according to claim 1, wherein said first region comprises an epitaxial layer.

5. The HVFET according to claim 1 wherein said buried region is connected to said substrate.

6. The HVFET according to claim 1 further comprising:

one or more additional buried regions of said first conductivity type within said first region and beneath said first surface.

7. The HVFET according to claim 1, further comprising an isolation diffusion region of said first conductivity type, said isolation diffusion region formed substantially beneath a second buried region within said substrate and substantially beneath said source diffusion region and said second region.

8. A high voltage FET comprising:

a semiconductor substrate of a first conductivity type having a substrate surface;

a first region of a second conductivity type within said semiconductor substrate and having a first surface, said first surface bordering said substrate surface;

a source electrode;

a source diffusion region within said substrate, said source diffusion region connected to said source electrode;

a drain electrode;

a drain diffusion region within said first region, said drain diffusion region connected to said drain electrode;

a buried region of said first conductivity type, said buried region formed within said first region and beneath said first surface, said buried region forming dual current channels within said first region with one channel above said buried region and one channel below said buried region;

an insulating layer over said substrate and said first surface; and

a gate electrode connected to a portion of said insulating layer residing over said substrate surface.

9. The HVFET according to claim 8, further comprising:

a second buried region, said second buried region substantially beneath said source diffusion region.

10. The HVFET according to claim 8, further comprising:

a second region of first conductivity type within substrate and adjacent said source diffusion region.

11. The HVFET according to claim 10, further comprising

a second buried region within said substrate and substantially beneath said source diffusion region and said second region.

12. The HVFET according to claim 8, wherein said first region comprises an epitaxial layer.

13. The HVFET according to claim 12, further comprising an isolation diffusion region of said first conductivity type, said isolation diffusion region formed substantially beneath said second buried region.

14. A high voltage FET, comprising:

a semiconductor substrate of a first conductivity type having a substrate surface;

a first region of a second conductivity type having a first surface, said first region within said substrate and said substrate surface bordering said first surface, said first region further comprising an above region and a below region;

between said above region and said below region, a buried region of a first conductivity type residing substantially across said first region and further across a section of said substrate, said section being beneath said substrate surface and adjacent said first region, said buried region comprising a plurality of openings

comprised of material from said first region, said openings connecting said above region to said below region to form conducting channels within said first region;

a source diffusion region of a second conductivity type within said substrate;

a source electrode connected to said source diffusion region;

a drain diffusion region of a second conductivity type within said substrate;

a drain electrode connected to said drain diffusion region;

an insulating layer formed over said substrate surface and said first surface; and

a gate electrode formed over a section of said insulating layer residing over said substrate surface and a section of said first surface.

15. The HVFET according to claim 14, wherein the number of openings in said buried region is two thereby enhancing current conduction within said first region.

16. A method of fabricating an extended drain region for a high voltage FET, comprising the steps of:

implanting, into a substrate of a first conductivity type using a dopant of a second conductivity type, a first region having a first surface, followed by diffusion; and

implanting a dopant of said first conductivity type using a high energy implant a buried region within said first region and underneath said first surface.

17. The method according to claim 16, wherein the buried region resides substantially between 1.0 to 2.0 microns beneath said first surface.

18. A method for fabricating a high voltage FET, comprising the steps of implanting and diffusing a substrate surface with a material of a first conductivity type to form a first region within said substrate and having a first surface which borders said substrate surface;

implanting, using a high energy implant, said first region with material of said first conductivity type to form a buried region beneath said first surface; and

implanting said first region with material of said first conductivity type to form a drain diffusion region, and implanting said substrate with material of said first conductivity type to form a source diffusion region.

19. The method according to claim 16, wherein said high energy implanting step uses a mask to form a second buried region into said substrate.

20. The method according to claim 16, further comprising the step of implanting said substrate with material of said first conductivity type to form a second region adjacent source diffusion region.

21. A high voltage FET comprising:

a semiconductor substrate of a first conductivity type having a substrate surface;

a first region of a second conductivity type having a first surface, said first region within said substrate, said first surface bordering said substrate surface;

a source diffusion region within said substrate;

a source contact connected to said source diffusion region;

a buried region of said first conductivity type within said first region and beneath said first surface, said buried region forming dual current channels within said first region, one channel above said buried region and another channel below said buried region;

a drain diffusion region of said second conductivity type, said drain diffusion region within said first region, and said drain diffusion region overlapping said buried region;

a drain contact connected to said drain diffusion region;

a gate region having an insulating layer formed over said substrate surface; and

a gate electrode on a section of said insulating layer over said substrate surface, said gate electrode overlapping said buried region, and said gate electrode

together with said insulating layer and said substrate forming an insulated gate having a transistor channel between said source and said first region.

22. The high voltage FET of claim 21 further comprising a second region of said first conductivity type adjacent said source diffusion region.

23. The high voltage FET of claim 21 further comprising a second buried region, said second buried region substantially beneath said source diffusion region.

24. A high voltage FET comprising:

a semiconductor substrate of a first conductivity type having a substrate surface;

a first region of a second conductivity type having a first surface, said first surface bordering said substrate surface;

a second region of said first conductivity type, said second region having a pair of channels coupled to said first region;

a source diffusion region within said substrate;

a source contact connected to said source diffusion region;

a buried region of said first conductivity type within said first region and beneath said first surface, said buried region forming dual current channels within said first region, one channel above said buried region and another channel below said buried region,

a drain diffusion region within said first region;

a drain contact connected to said drain diffusion region;

a gate region having an insulating layer formed over said substrate surface; and

a gate electrode on a section of said insulating layer over said substrate surface, said gate electrode together with said insulating layer and said substrate forming an insulated gate having a transistor channel between said source and said first region.

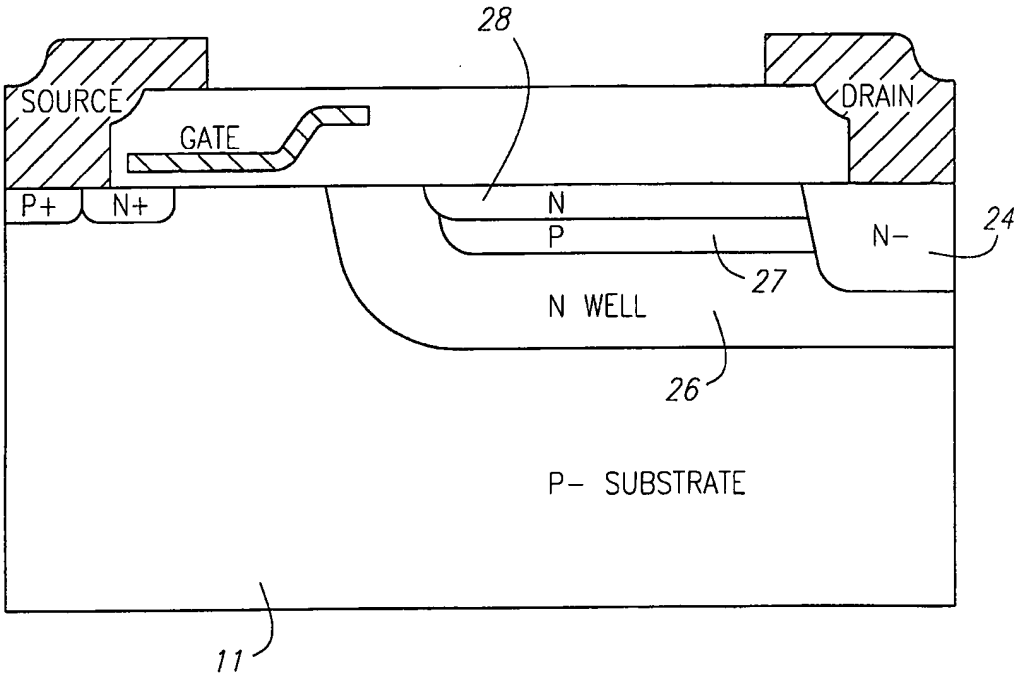


FIG. 1

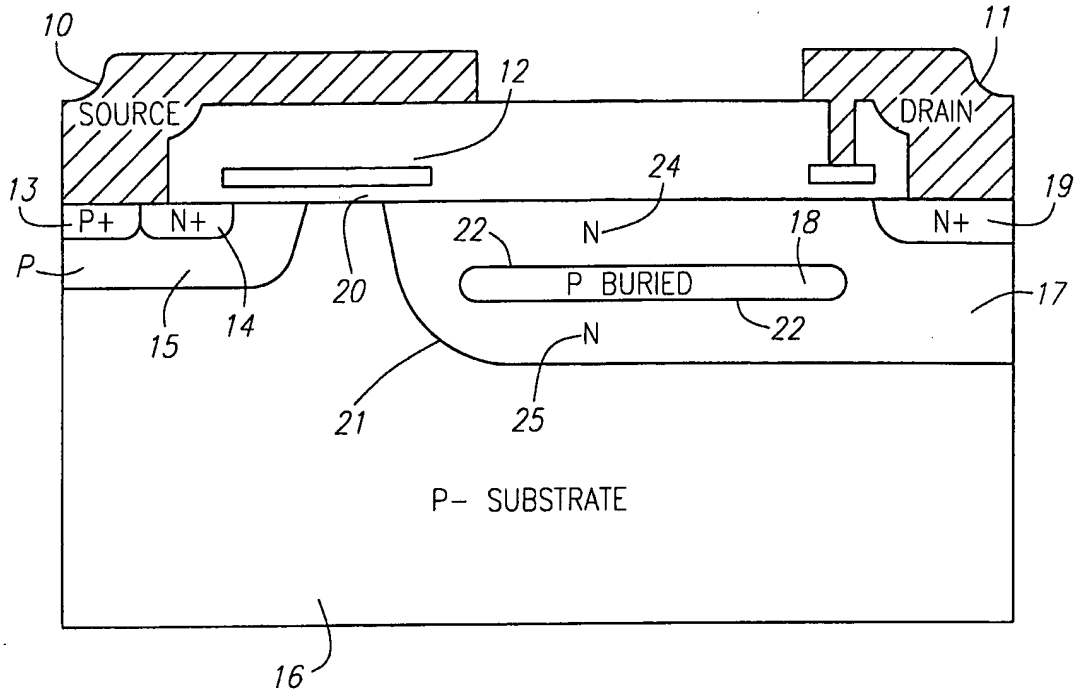

10
11
12
SOURCE
DRAIN
13
24
19
P+
N+
N
18
N+
22
P
P BURIED
17
20
22
15
14
N
21
25
P- SUBSTRATE
16

FIG. 2

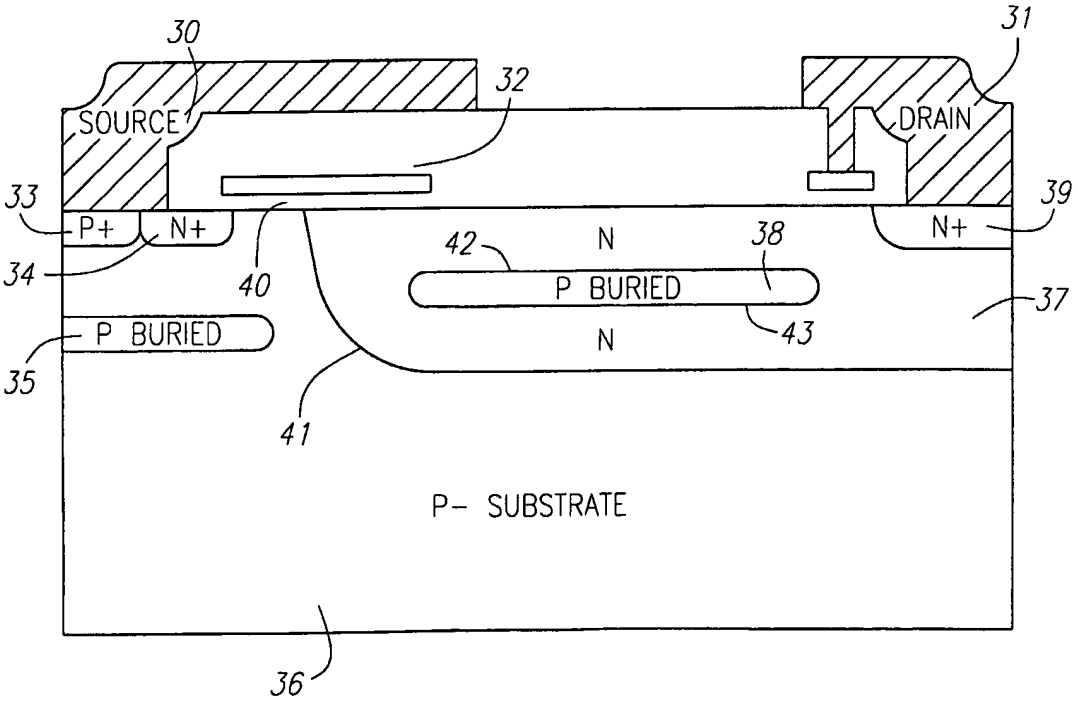

30
31
32
SOURCE
DRAIN
33
39
P+
N+
42
N
38
34
40
P BURIED
37
P BURIED
43
N
35
41
P- SUBSTRATE
36

FIG. 3

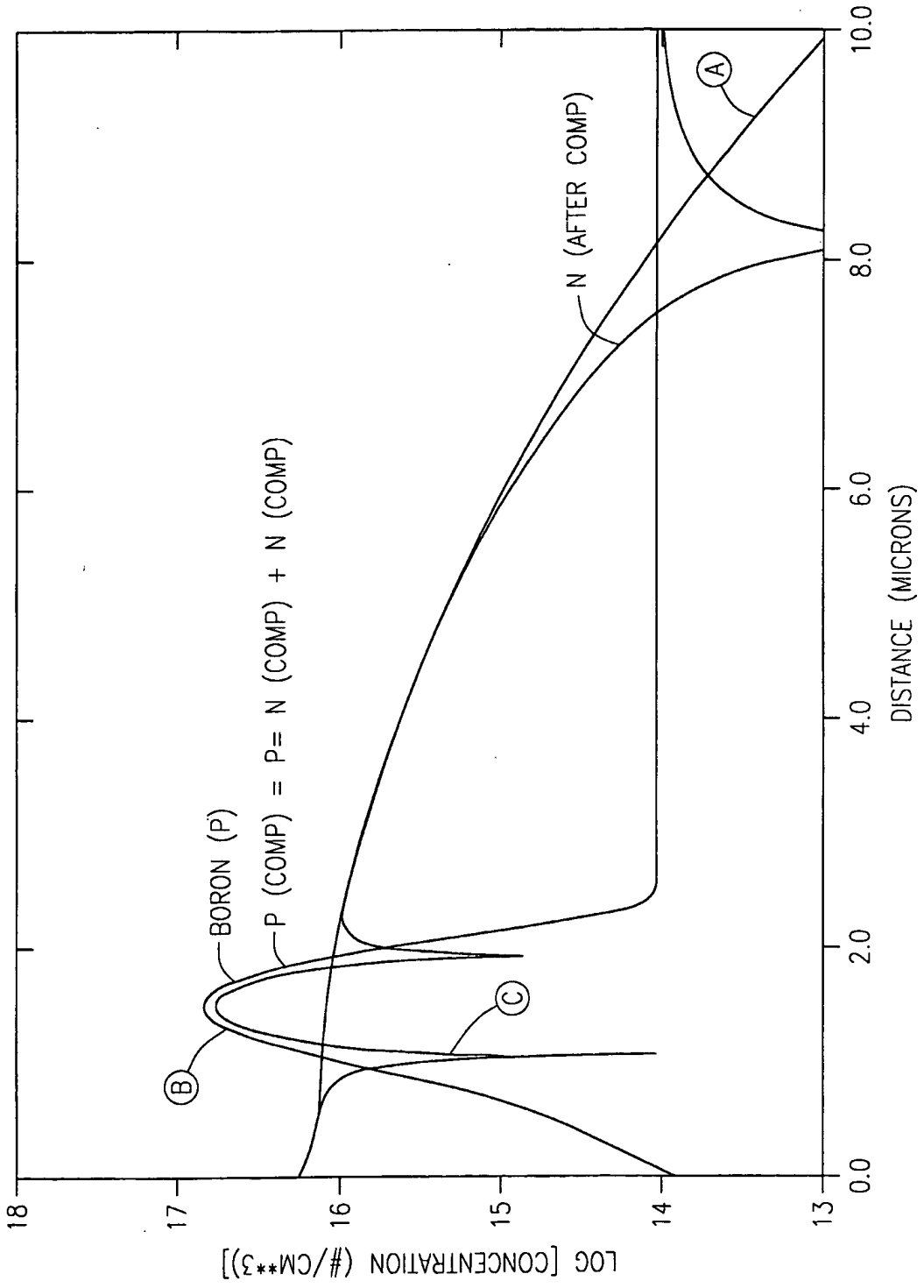

LOG [CONCENTRATION (#/CM**3)]
18
17
16
15
14
13
0.0
2.0
4.0
6.0
8.0
10.0
DISTANCE (MICRONS)
N (AFTER COMP)
P (COMP) = P= N (COMP) + N (COMP)
BORON (P)
A
B
C

FIG. 4

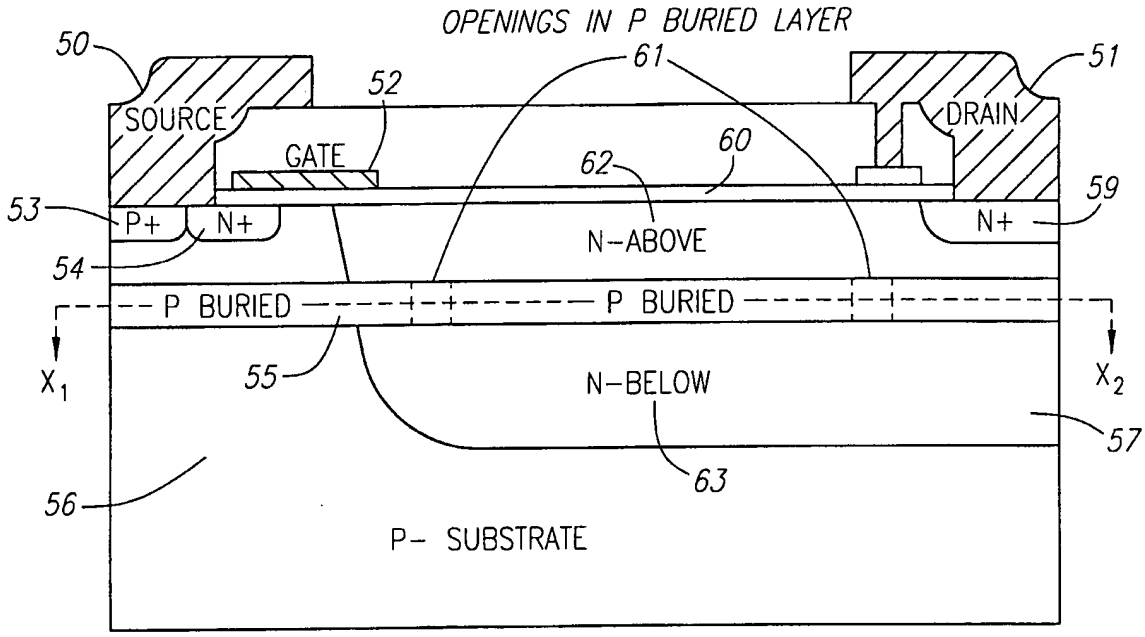

OPENINGS IN P BURIED LAYER
50
61
51
52
SOURCE
DRAIN
GATE
60
62
59
53
P+
N+
N+
N-ABOVE
54
P BURIED
P BURIED
X1
55
N-BELOW
X2
57
63
56
P- SUBSTRATE

FIG. 5

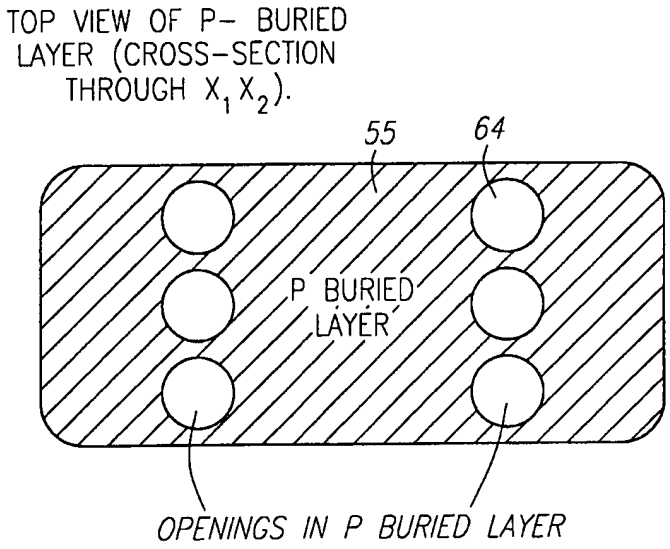


FIG. 6

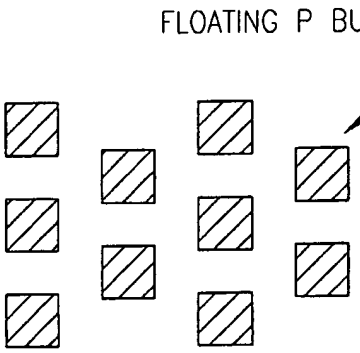


FIG. 7

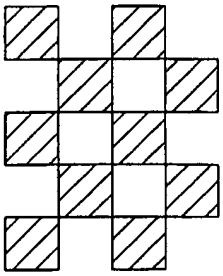


FIG. 8

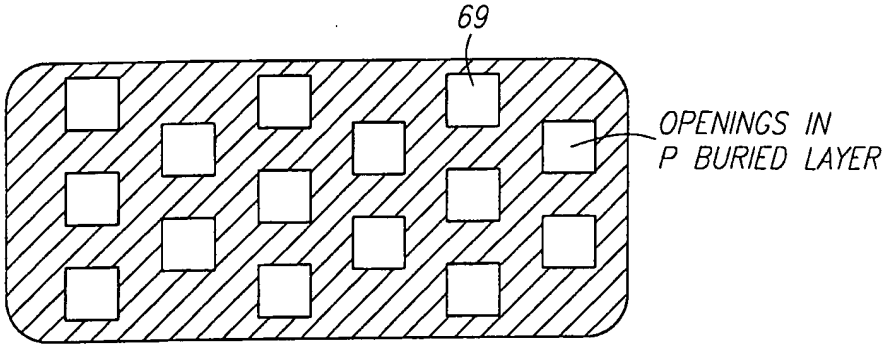


FIG. 9

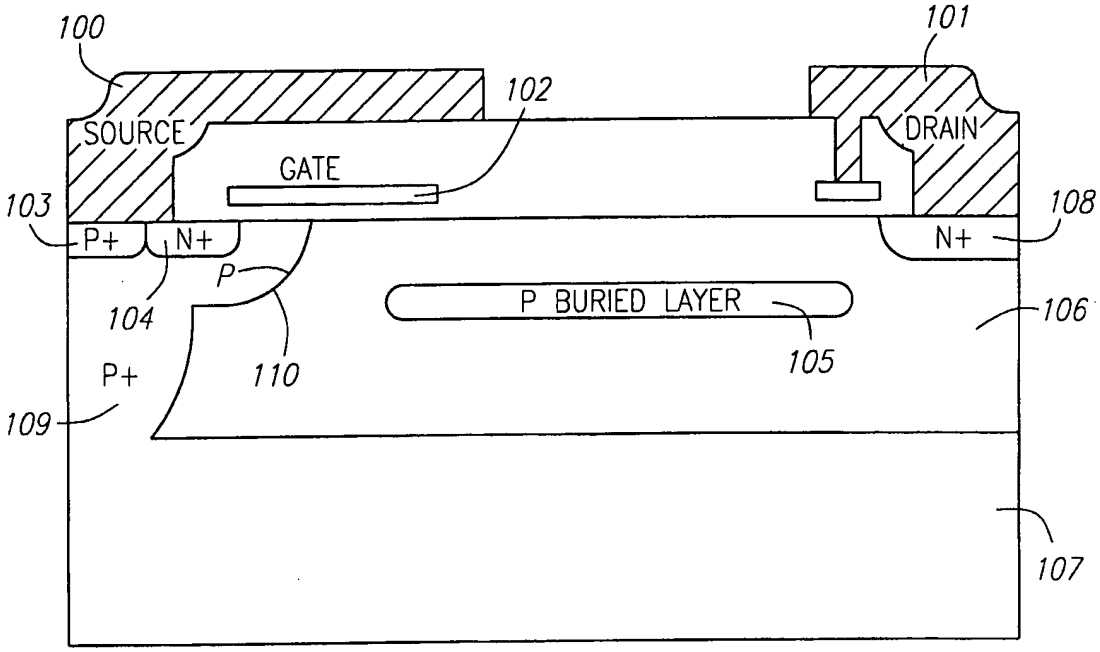

100
101
102
SOURCE
DRAIN
GATE
103
108
P+
N+
N+
P
104
P BURIED LAYER
106
105
P+
110
109
107

FIG. 10

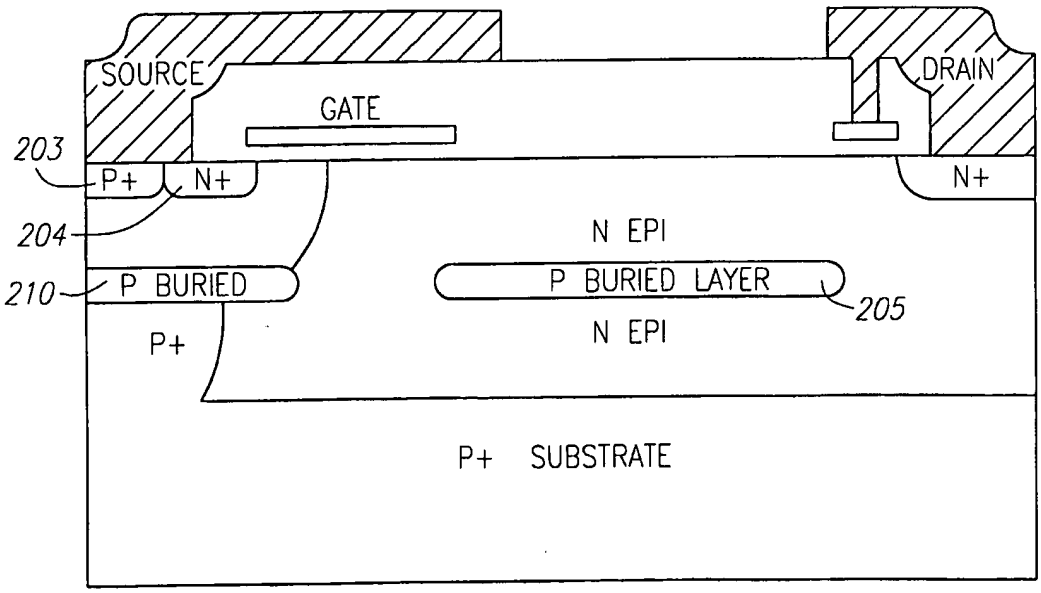

SOURCE
DRAIN
GATE
203
P+
N+
N+
204
N EPI
210
P BURIED
P BURIED LAYER
205
P+
N EPI
P+ SUBSTRATE

FIG. 11

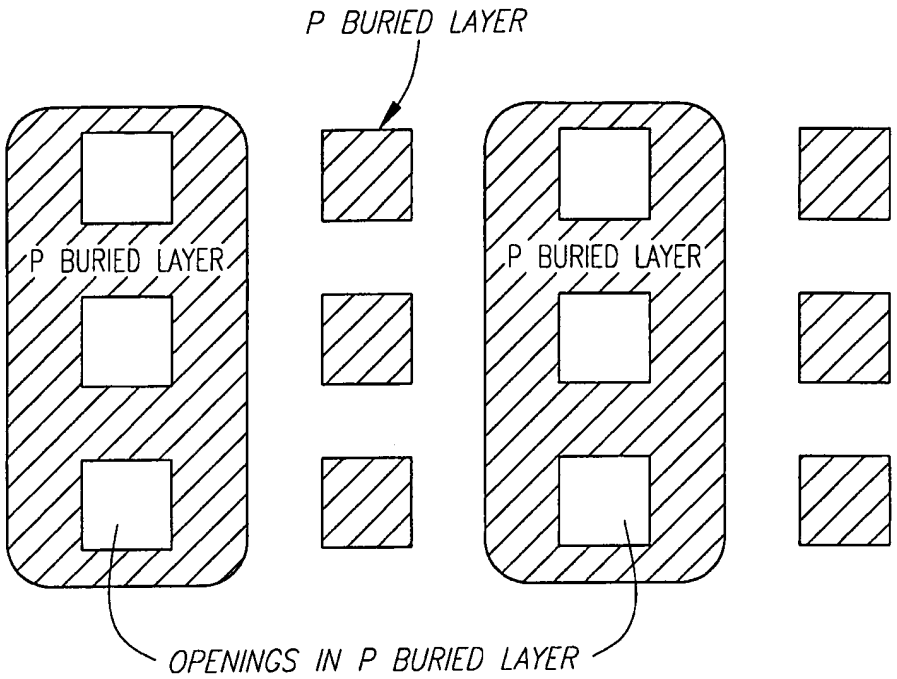
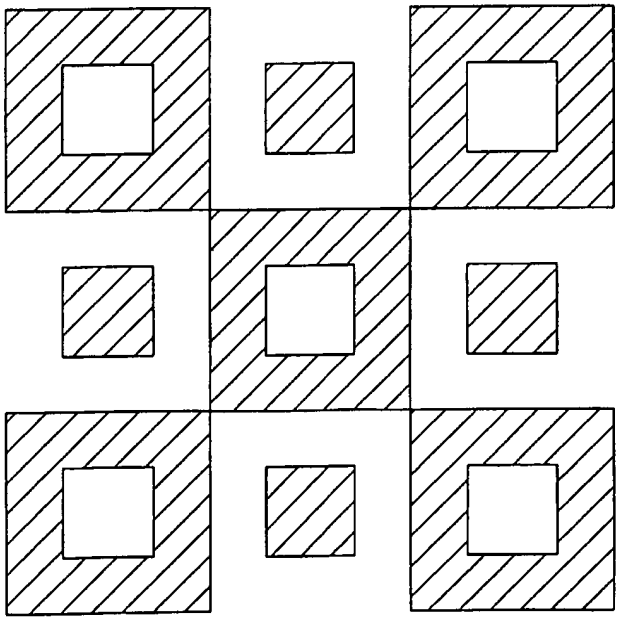


FIG. 12A



SHADED REGIONS REPRESENT
P BURIED LAYER

FIG. 12B

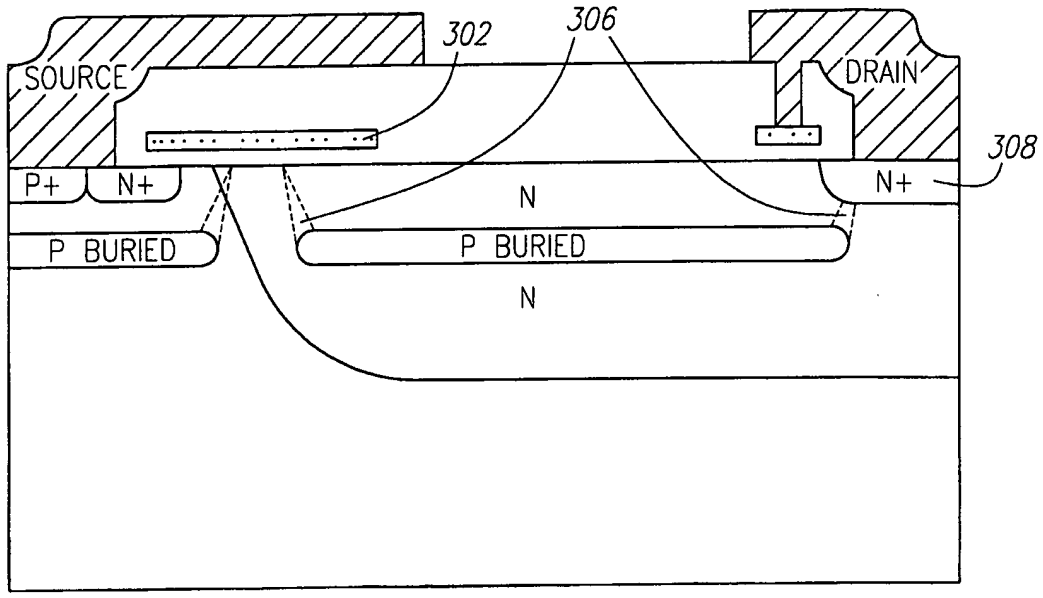

SOURCE
302
306
DRAIN
308
P+
N+
N
N+
P BURIED
P BURIED
N

FIG. 13

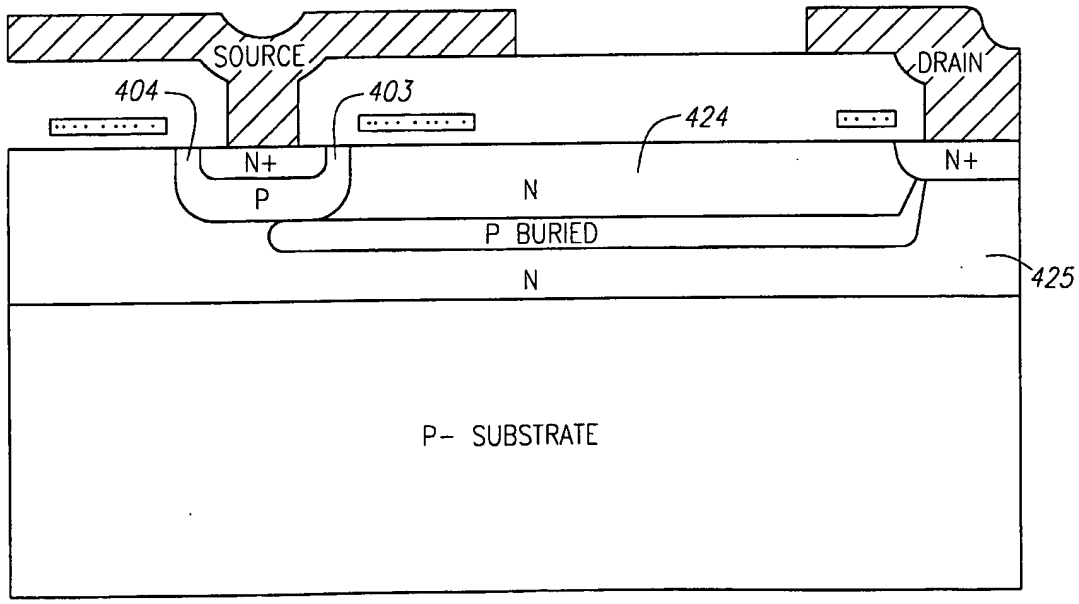

SOURCE
DRAIN
404
403
424
N+
N+
P
N
P BURIED
N
425
P- SUBSTRATE

FIG. 14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/17637

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L29/78 H01L29/10 H01L21/336

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 155 574 A (YAMAGUCHI HIROSHI) 13 October 1992 see column 8, line 15 - line 29; figure 7	1,2,4,6, 8,10,12, 14,15,24 1-4,6,8, 10,12, 21,22,24
Y	US 5 313 082 A (EKLUND KLAS H) 17 May 1994 cited in the application see the whole document	1-4,6,8, 10,12, 21,22,24
X	US 4 626 879 A (COLAK SEL) 2 December 1986 cited in the application see the whole document	1-4,8

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 1998	27/01/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Mimoun, B

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 97/17637

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category '	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 521 105 A (HSU CHING-HSIANG ET AL) 28 May 1996 see abstract	16-20
Y	US 5 359 221 A (MIYAMOTO MASAFUMI ET AL) 25 October 1994 see abstract; figures	16-20
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 590 (E-1628), 10 November 1994 & JP 06 224426 A (MATSUSHITA ELECTRON CORP), 12 August 1994, see abstract	1,5
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 347 (E-1240), 27 July 1992 & JP 04 107867 A (MATSUSHITA ELECTRON CORP), 9 April 1992, see abstract	1,5
A	DE 43 09 764 A (SIEMENS AG) 29 September 1994 see abstract; figures 2-7	1,6
A	US 4 922 327 A (MENA JOSE G ET AL) 1 May 1990 see abstract; figures	7

3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 97/17637

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